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7 Series FPGAs Data Sheet: Overview

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Product Specification

General Description

The 7 series FPGAs offer the highest performance and bandwidth for demanding applications, ranging from low cost, small form factor, cost-sensitive, high-volume applications to the most demanding high-performance, high-bandwidth, high-logic capacity, and high-DSP capacity applications.

- Spartan® 7 Family: Optimized for low power, cost, and bandwidth
- Artix® 7 Family: Optimized for low power and high performance for cost-sensitive applications
- Kintex® 7 Family: Optimized for high performance and cost-sensitive applications
- Virtex® 7 Family: Optimized for highest system performance and capacity
- Zynq® 7000 All Programmable SoC: Integrates the industry's leading ARM® dual-core Cortex®-A9 MPCore™ processor based processing system (PS) and 7 series programmable logic (PL) in a single device
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Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic is based on the 28 nm, high-performance, low-power, low-voltage, high-k dielectric and metal gate high-performance 1 (HP) process technology.
- Stacked silicon interconnect (SSI) technology enables the industry's highest bandwidth, highest logic capacity, and highest DSP capacity FPGAs.
- Extensive clock management with up to 24 clock regions, 32 global clock lines, up to 16 per clock region, and up to 12 phase-shifted clocks per clock region.
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- Dedicated, low-latency, high-performance DSP slices with 25 x 18 two's complement multiplier/accumulator, 48-bit accumulator, and pre-adder.
- Dedicated, low-power, 36 Kb and 18 Kb block RAM resources with up to 72 bits wide, 2 ports per block.
- Dedicated, high-speed, 12 bit, 1 GS/s and 1 MS/s, 64 channel, multi-channel analog-to-digital converter (XADC) with on-chip thermal and power supply sensors

LC tank or, in the case of the GTZ, a single LC tank architecture to allow the best blend of flexibility and performance while minimizing board space and component count. The GTP supports up to 6.6 Gb/s, the GTX supports up to 12.5 Gb/s, the GTH supports up to 13.1 Gb/s, the GTP operates up to 6.6 Gb/s, the GTX operates up to 12.5 Gb/s, the GTH operates up to 13.1 Gb/s, and the GTZ operates up to 28 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The serial transmitter and receiver are differential 2-level pulse amplitude modulation (2PAM) capable. The transmitter and receiver can also contain programmable numbers up to 165 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

The transceiver fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80. Additionally, the GTZ transceiver supports up to 160:16 bits and 80:16. This allows the designer to trade off datapath width for rising margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. The GTP, GTX, and GTH transceivers can optionally invert the polarity of the transmitted signal to simplify the routing of the internal traps. The incoming parallel data to be transmitted can optionally be encoded and/or scrambled to support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal is transmitted at a user-defined multiple of the reference clock frequency. The transceiver operating as well as programmable pre- and post-emphasis to compensate for PC-board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, such 16, 20, 32, 40, 64, or 80 bits. Additionally, the GTZ receiver supports up to 160:16 and 80:16. This allows the FPGA designer to trade off internal datapath width versus logic timing margin. The receiver takes the incoming bit-serial data and uses a clock-and-data recovery (CDR) to recover the embedded timing information (relative to the local and other interconnect characteristics), and uses the reference clock signal to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees transitions. The receiver can optionally automatically correct the polarity of the incoming data. The receiver can also bypass the RX\u\DFE\u\CDR. For short channels, the transceivers offers a special low power mode (LPM) to reduce power consumption by approximately 30%.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver when a high-speed link is not established. The GTP, GTX, and GTH transceivers use the link in a powered-down state or has not yet been initialized. This benefits PCI Express and SATA/SAS applications.

Integrated Interface Blocks for PCI Express Designs

Highlights of the integrated blocks for PCI Express include:

- Compliant to the PCI Express Base Specification 2.1 or 3.0 (depending of family) with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s), Gen2 (5 Gb/s), and Gen3 (8 Gb/s) depending on device family
- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC Advanced Error Reporting and EZ\u\Retry
- Multiple function and single root I/O virtualization (SR-IOV) support enabled through sub-logic wrappers or embedded in the integrated block depending on family

All 7 series FPGAs, Zynq-7000 AP SoCs, and Zynq UltraScale+ MPSoCs have at least one integrated block for PCI Express technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1 or 3.0. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom PFGA logic to PCIe communication via the PCI Express protocol, and to attached AXIP Endpoint devices, such as Ethernet Controllers or Flash Memories, to the FPGA.

This block is highly configurable to system design requirements and can operate 1, 2, 4, or 8 lanes at the 2.5 Gb/s, 5.0 Gb/s, and 8.0 Gb/s data rates. For high performance applications, advanced buffering techniques of the block offer a flexible

maximum payload size of up to 1 024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serialized transmission, to the block RAM resources for buffering, and to internal fabric resources when implemented. Power Gate, Clock Gate, Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block, block RAM, and GTP transceivers) together and adds the logic needed to complete the PCI Express solution. The system designer has control over many configurable parameters: lane width, maximum payload size, FPGA logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Xilinx offers two wrappers for the integrated block. AXI-Stream and Block wrappers are available that layer TRN/Local Link is not available in 7 series devices for the integrated block for PCI Express. AXI-Stream is recommended for customers migrating from Virtex-6 or Spartan-6 designs using TRN/Local Link. The Block wrapper is primarily megawiz\u\ed to designed for Xilinx Platform DoCM/DoM design flow and MicroBlaze™ processor based designs.

More information and documentation on solutions for PCI Express designs can be found at: http://www.xilinx.com/products/technology/pci-express.htm

Configuration

There are many element configuration features, including:

- High-speed SPI and BPI (parallel NOR) configuration
- Bitstream encryption and authentication
- 256-bit AES encryption with HMAC/SHA-256 authentication
- Built-in SEU detection and correction
- Partial reconfiguration

The 7 series FPGAs store their customized configuration in SRAM-type internal latches. There are up to 450 Mb configuration bits, depending on device size and user-design implementation options. The configuration storage is volatile and requires that the FPGA be configured at power-on and reconfigured after power-down. The FPGA offers a flexible, PROGRAM_B pin only. Several methods and data formats for loading configuration are available, determined by the device mode and pin strapping.

The SPI interface (x1, x2, and x4 modes) and the BPI interface (parallel NOR x8 and x16) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself. The FPGA automatically detects the bus width on the fly, eliminating the need for external logic to control the configuration interface. The FPGA drives the CCLK output pin, the clock for SPI. The larger bus width\u increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on. Some configuration options such as BPI are not supported in all device package combinations. Refer to UG470, 7 Series FPGAs Configuration User Guide for details.

In master mode the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of master configuration. Master SPI mode and x1 BPI modes up to 32 bits wide are also supported by the FPGA that are especially useful for process-driven configuration.

The FPGA has the ability to reconfigure itself with a different image using SPI or BPI flash, eliminating the need for an external controller. The FPGA can reload its bitstream at any time and in any order. Users can initiate reconfiguration from an operational FPGA at the end of the process. This is especially useful for updates to a design after the end product has been shipped. For example, a communications system can be updated remotely with a new feature set or bug fixes without a truck roll or technician visit. This feature allows customers to keep their end users current with the most up-to-date designs while the product is already in the field.

Partial reconfiguration port (ZPR) gives the system designer easy access to the configuration and status registers of the ARM/CM\u\FU, AES/SHA\u\encryption/decryption/authentication, CRC, frame ECC, and frame and memory mapped registers, accessing and modifying block-specific configuration bits as well as status and control registers.

Encryption, Readback, and Partial Reconfiguration

The 7 series FPGA bitstream supports AES-256 encryption, authentication, which contains sensitive customer IP, can be protected with 256-bit AES encryption and HMAC/SHA-256 authentication to prevent unauthorized copying of the design. The FPGA performs decryption on the fly during configuration using an internally stored 256-bit key. This key can reside in battery-backed RAM or in nonvolatile eFUSE bits.

Most configuration data can be read back without affecting the system's operation. Typically, configuration is an uninterruptible process, but the FPGA can optionally support partial reconfiguration. Readback capture is a powerful flexible feature that allows the user to change portions of the FPGA while other portions continue to operate. Users can store these portions to RI more SP into smaller devices, saving cost and power. Where application in certain designs, partial reconfiguration can greatly improve the versatility of the FPGA.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible analog-to-digital configuration analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to XDC measurements
- The XADC supports 17 external analog inputs (16 VP/VN) integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the 7 series FPGAs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/xadc

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to convert a single channel or a maximum of 16 channels. The ADCs can also be configured to convert a fixed or a user-defined sequence of signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 300 KHz at sample rates of 1MSPS. It is possible to support higher analog bandwidths using external analog multiplexer circuitry. Refer to UG480, 7 Series FPGAs and Zynq-7000 AP SoC and Zynq UltraScale+ MPSoC Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide.

The XADC optionally uses an on-chip reference circuit (+1%), thereby eliminating the need for any external active reference. The XADC can also operate with an external reference. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

If the XADC is not instantiated in a design, then by default it digitizes the output of all on-chip sensors. The most recent measurements of chip temperature and power supply voltages are stored in dedicated registers for access at any time. Alternatively, the XADC can be configured to monitor a user-specified sequence of the on-chip sensors and unipolar/bipolar analog inputs. A user-specified limit (for example, 100°C) can be used to initiate an automatic power/thermal

7 Series FPGA Ordering Information

Table 12 shows the speed and temperature grades available in the different device families. Some devices might not available in every package and temperature range.

Table 12: **7 Series Speed Grade and Temperature Ranges**

Device Family	Devices	Speed Grade, Temperature Range, and Operating Voltage			
		Commercial (C) 0°C to +85°C	Extended (E) 0°C to +100°C	Industrial (I) –40°C to +85°C	Extended (E) –40°C to +100°C
Spartan-7	A7	–1L (0.95V)	–1L (0.95V)	–1L (0.95V)	–1L (0.95V)
		–2L (0.95V)	–2L (0.95V)	–2L (0.95V)	
		–1 (1.00V)	–1 (1.00V)	–1 (1.00V)	
				–1Q (1.00V)[1]	
Artix-7	A35	–3L (0.95V)	–3L (0.95V)	–3L (0.95V)	
		–2L (0.95V)	–2L (0.95V)	–2L (0.95V)	
			–2LE (1.00 or 0.95V)		
		–2 (1.00V)	–2 (1.00V)	–2 (1.00V)	
				–2I (1.00V)	
	A50	–3L (0.95V)		–3L (0.95V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
Kintex-7	K70T	–3L (0.95V)	–3L (0.95V)	–3L (0.95V)	
			–2LE (1.00 or 0.95V)		
	K70, K70T, K70F, K70TF, K70HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)	–2L (0.95V)	–2L (0.95V)	
		–2 (1.00V)	–2 (1.00V)	–2 (1.00V)	
				–2I (1.00V)	
	K160T, K160F, K160TF, K160HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
	K325T, K325TF, K325HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
	K410T, K410TF, K410HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
Virtex-7 T	K420T, K420TF, K420HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
	K580T, K580TF, K580HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
	K690T, K690TF, K690HT	–3 (1.00V)		–3 (1.00V)	
		–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
Virtex-7 HT	H580T	–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
	H580T, H580HT	–3 (1.00V)		–3 (1.00V)	
	H680T, H680HT	–3 (1.00V)		–3 (1.00V)	
	H682T	–2 (1.00V)		–2 (1.00V)	
Virtex-7 XT	H580T	–2L (0.95V)		–2L (0.95V)	
		–2 (1.00V)		–2 (1.00V)	
	H580T, H580HT	–3 (1.00V)		–3 (1.00V)	
	H680T, H680HT	–3 (1.00V)		–3 (1.00V)	
	H682T	–2 (1.00V)		–2 (1.00V)	

The Spartan-7 FPGA ordering information is shown in Figure 1. Refer to the Package Marking section of UG475, 7 Series FPGAs Packaging and Pinout for a more detailed explanation of the device markings.